Circuit Design for Green Communications – Methods, Tools and Examples

Galia Marinova
Technical University Sofia, gim@tu-sofia.bg

Zdravka Tchobanova
Technical University Sofia, z.chobanova@tu-sofia.bg

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Galia Marinova[1], Zdravka Tchobanova[1]

[1]Technical University-Sofia, Faculty of Telecommunications,
8, bul. "Kliment Ohridski", Sofia-1000, Bulgaria
{gim, z.chobanova}@tu-sofia.bg

Abstract. The paper makes an overview of the existing methods applied for circuit design with low power consumption objective. It considers Computer-Aided Design (CAD) tools and modules for power consumption estimation at the design stage. For analog and mixed analog-digital circuit design, the power estimation options in ORCAD Design Suit with PSpice and Analog Filter Wizard are studied. For digital communication systems the study covers the power estimation, analysis and optimization in ISE and Vivado systems, Xilinx Power Estimator (XPE) tool and spreadsheet, the XPower Analyzer, as well as similar tools proposed by ALTERA - PowerPlay Early Power Estimator and QUARTUS II Power Play Power Analyzer. Two examples are developed: Power consumption estimation of a Universal Software Radio Peripheral (USRP)-based communication system design, based on datasheets and software energy monitoring tools, and power consumption estimation of a Kasami pseudo-random sequence generator circuit design on FPGA using Vivado.

Keywords: Low Power Consumption, CAD tools, Power Estimation, FPGA, USRP, Analog and Analog-Digital Circuits

1. Introduction

Low power consumption is an important objective in green communications, which has to be taken in consideration as early as possible at the design stage. It's also a criterion for the selection of solution and technology for a given application. The paper considers methods and tools that can help circuit designers to develop green design for communications. The outline of the paper is: First an overview is made of the methods for power estimation and low power design in communications, then tools for power estimation in CAD systems and Software energy monitoring tools are studied with application for analog, analog/digital and digital circuits on FPGA and USRP platforms; Two examples of power estimation for design on FPGA and USRP-based design are developed to illustrate the application of different tools for power estimation; At the end there concluding remarks and plans for future research are given.

2. Methods for Power Estimation and Low Power Circuit Design in Communications - state-of the art

Here are noted low power design solutions for different hardware realizations, proposed in scientific literature. Methods and approaches provided in literature are based on temperature

estimation and relocation of processing elements from hot spots to cool spots on FPGA, switching between different radio standards, parametrization and Dynamic and partial reconfiguration of FPGA, VHDL and Verilog coding for low power consumption and development of domain specific reconfigurable processor.

Authors in [1] start with the definition of total power consumption in an FPGA as:

$$Pt = Pst + Psc + Pdy , \quad (1)$$

where Pt is total power, Pst is static power, Psc is short-circuit power and Pdy is dynamic power, the predominance being of dynamic power. The authors propose to measure local temperature in the chip by sensor system (array of temperature sensors embedded in the FPGA) which measures the temperature at different locations on the FPGA and high temperature spots are identified. The method is illustrated on Virtex-5 FPGA with ML550 board (Xilinx). Autors demonstrate that power consumption can be decreased through moving processing elements from hot spots at low temperature spots and through design area reduction.

In paper [2] the authors compare 3 methods of hardware realization of elements in software defined radio – Velctro approach (based on switching between different radio standards using a multiplexor), Parametrization approach (including parametric tuning of any function) and FPGA Dynamic and Partial Reconfiguration (DPR), where part of the system is reprogramed while the rest of the system is running. The comparison is estimated for a convolutional coder circuit with r=1/2 and K=3 and DPR approach is pointed as giving the lowest power consumption of the design.

The authors of paper [3] describe the design of a 4-bit asynchronous counter, developed in Xilinx ISE 14.2 and implemented on Virtex-6 FPGA, XC6VLX250T with ML605 development board. The power consumption is estimated through XPower 14.2. Two types of coding are compared – mapping the *clock enable* to the control port (Verilog and VHDL codes are proposed) and to the LUTs. The second design gives a lower power consumption estimate and the reduction obtained is 6%. This is due to the different number of LUTs, D flip-flops, clock buffers and IO buffers, the power consumption being proportional to the number of elements used for the realization of the HDL on the FPGA.

Paper [4] is focused on the implementation of cryptographic algorithms with public key. A domain-specific reconfigurable cryptographic processor (DSRCP) is developed. The analysis shows that only 5% of the total power is used for useful processing and 65% is dissipated in the programmable connection. DSRCP is 2 to 3 times more energy effective than the software solutions or FPGA solutions, Xilinx XC4000 is used for comparison. Some basic instructions for low power VLSI chip design are proposed in [15].

3. Tools for Power Estimation in CAD Systems and Software Energy Monitoring Tools

There are several papers on green communications emphasizing on their importance and concluding with advices for appropriate policies. A study on tools for power estimation is performed to help low power design and optimization.

3.1. Power Estimation and Optimization in CAD Systems for Analog and Analog-Digital Design

An estimation of power dissipation in analog and analog-digital circuit designs can be obtained in Cadence ORCAD/PSpice simulator [6] through the *Operating point analysis* and the results are listed in the output file as Total power dissipation in Watts.

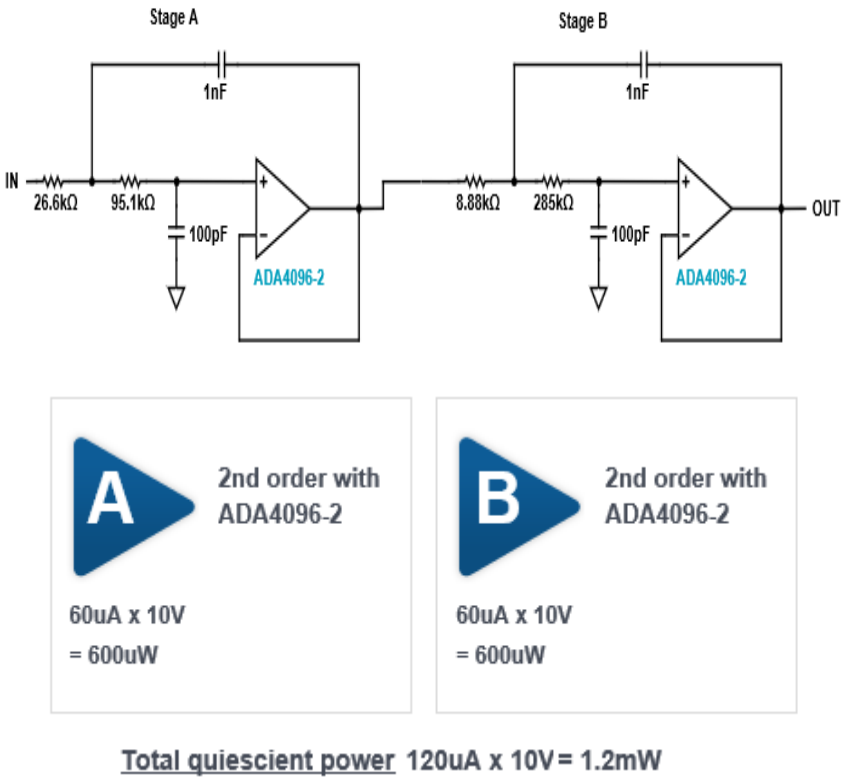

Fig.1. Low pass filter realization in Analog Filter Wizard tool and results from power estimation in the tool

Other analog design tool that provides power estimation options is Analog Filter Wizard of Analog Device [7]. Figure 1 illustrates Low pass filter realization in Analog Filter Wizard tool and results from power estimation in the tool. The quiescent power consumption of the filter is calculated. The input signal which can have a significant impact on power consumption is not modeled. The tool offers an option for Low power optimization, as well. The quiescent power consumption of the example from Fig.1 is 1.2mW.

3.2. Tools for Power Estimation and Analysis in FPGA-Based Digital Circuit Design

The serious focus of circuit designers on green communications design and more specifically on low power design has influenced FPGA providers, as Xilinx, to develop Power efficiency and management strategies and to consider e FPGA Performance-Per-Watt Metric for new low power device families. The main estimates on FPGA are based on Worst-Case Power Analysis. The impact of the implementation of different FPGA families for a single design can be studied using Xilinx Power Estimator (XPE) tool [13]. Thermal analysis, system packaging and need of heatsinks, which are closely connected to power consumption analysis, are also considered.

FPGA providers propose two kind pf tools for low power design – the power estimators and the power analyzers which are options in the development tools. The principal features and of these tools are given further.

Xilinx Power Estimator (XPE) is an Excel based online tool offered by Xilinx for early determination of power and cooling specifications in FPGA designs. It's based on Worst case power analysis and it's integrated with ISE and Vivado suits. Calculators are provides for different device families (UltraScale+™, UltraScale™, 7 Series and Zynq-7000, Virtex-5 and Virtex-6, Spartan-3A/3AN/3A DSP and Spartan-6, Spartan-3E, Spartan-3, Virtex-4). Family, device and package are selected for a given project, environment parameters are defined and a Summary of *Total-On chip power, Junction Temperature, Thermal margin* and *Effective θJA* are calculated, graphs of *On-chip power per function*, *On-chip typical versus Maximal power*, *On-chip power over Vccint, On-Chip power over Junction temperature* and *Static current by supply* are drawn.

Xilinx power analyzer is an option in both ISE and VIVADO tools. The On-chip power is calculated with confidence level. Both ISE and VIVADO propose similar estimations. In VIVADO an additional graphical presentation is added.

PowerPlay Early Power Estimators (EPE) and QUARTUS Prime PowerPlay Power Analyzer are the tools provided by ALTERA [14] for power consumption estimation of designs on ALTERA FPGAs. EXCEL based estimators accompanied with user guides for different ALTERA device families (Statix, Cyclone, Arria, MAX) are downloadable. Besides the input data for the family, device, package and environmental parameters, a selection of power regulator is proposed. Static and total power, are calculated, as well as power per function. No graphs are available.

3.3. Software Energy Monitoring Tools

Software energy monitoring tools are used for estimating the real power consumption. They give information about the load of computer components in percent or the energy consumption by different components.

Microsoft Joulemeter [9] is such a tool in Windows OS and it gives information about the power consumption by different components and applications. When such a tool is run the changes in power consumption can be followed in real time in the panel Component Power Usage (Watts), where a running application or software program to be followed can be selected. Its name is written in the Application Power panel (CPU only). Bellow its power consumption is given as shown on Fig.2. This information can be saved in a file.

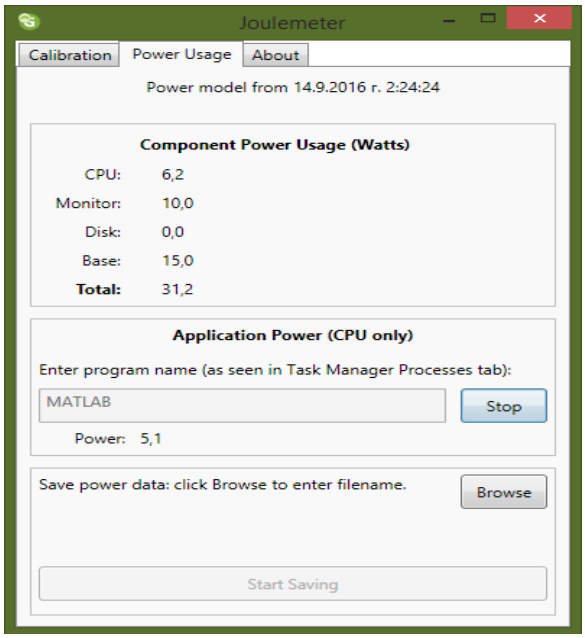

Fig.2. MS Joulemeter screen

In Linux OS similar tool can be started from the terminal. For example the command *top* gives an information for: process ID (PID), effective user name of process owner(USER), priority (PR), the percentage of the CPU (% CPU) and the memory (% MEM), the accumulated CPU time (TIME +), the name of the executable file (COMMAND) as shown on Fig.3.

```
top - 16:10:40 up 7 min,  2 users,  load average: 0.43, 0.64, 0.36
Tasks: 461 total,   2 running, 459 sleeping,   0 stopped,   0 zombie
%Cpu(s):  7.0 us,  7.0 sy,  0.0 ni, 85.8 id,  0.2 wa,  0.0 hi,  0.0 si,  0.0 st
KiB Mem:   3068416 total,  1565260 used,  1503156 free,    80940 buffers
KiB Swap:  3142652 total,        0 used,  3142652 free.   690500 cached Mem

  PID USER      PR  NI    VIRT    RES    SHR S  %CPU %MEM     TIME+ COMMAND
 3259 zdr       20   0 1012336  87188  30680 S  44.2  2.8   0:01.33 python2
```

Fig.3. Information generated by the command top in Linux OS

4. Examples of Power Estimation in Communication Circuit Design

Two examples are developed and presented to illustrate the application of different tools for power estimation of designs implemented on FPGA and USRP platforms.

4.1. Estimation of the power consumption of a Kasami random bit generator circuit

The circuit studied is Kasami pseudo-random sequence generator [5] defined by the polynomial of degree 10:

$$f(x)= x^{10}+x^3+1 \qquad (2)$$

with m'= 011 and k'=011.

The length of the pseudo-random suit of the circuit is 1023 bits. The electrical circuit of this Kasami pseudo-random sequence generator is presented on Fig.3. The circuit is described in VHDL and then simulated in Vivado 2014. The simulation results are presented on Fig.4 where *s* is the output signal. There the pseudo-ransom bit sequence is generated. In VHDL code D flip-flops are with additional Reset entry. Then the Kasami circuit is implemented on XC7Z020CLG484-1 circuit. Fig.5. shows the post-implementation utilization and Fig 6 shows the schematic generated in Vivado. Fig. 7 shows the results from the power analysis of Kasami pseudo-random sequence generator implemented on XC7Z020CLG484-1 circuit. The total on-chip power is 0.553 W. The Junction temperature is 31.4ºC and the Thermal margin is **53.6**ºC (4,5W). The confidence level of this estimation is considered as low. There is a repartition of the dynamic and static on-chip power, as well as reparation of on-chip power for signals, Logic and Intut/Output. The results confirm the predominance of dynamic power which is 77%. The part of power for Input/Output is the most considerable – 94%.

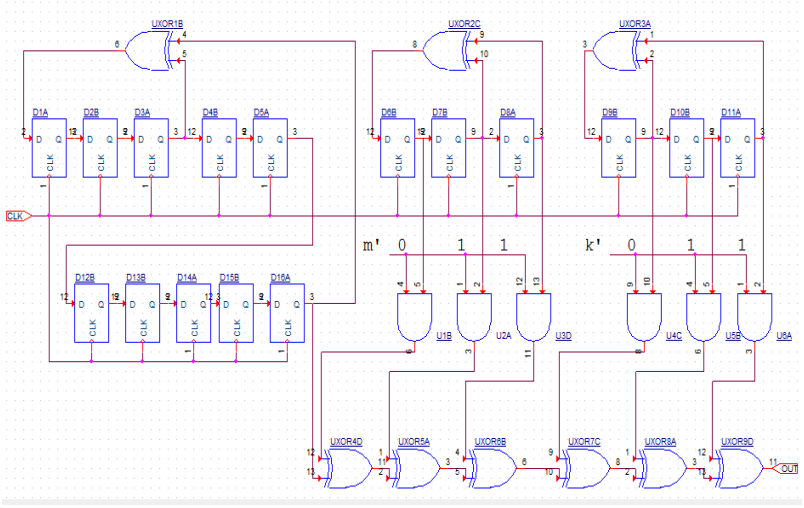

Fig.3. Electrical circuit of Kasami pseudo-random sequence generator

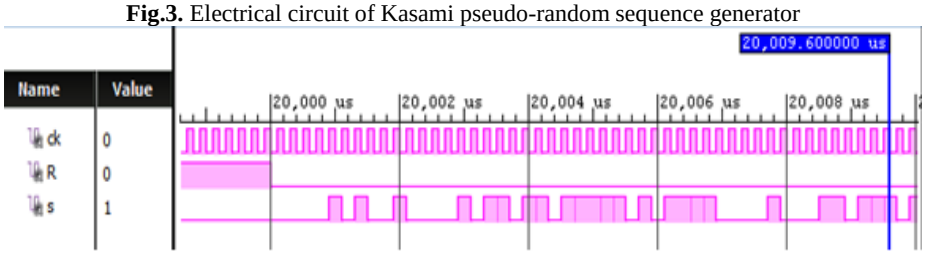

Fig.4. Timing diagrams of Kasami pseudo-random sequence generator from Fig.3, after simulation in Vivado 2014 of its VHDL description; *s* is the output signal where the pseudo-random sequence is generated

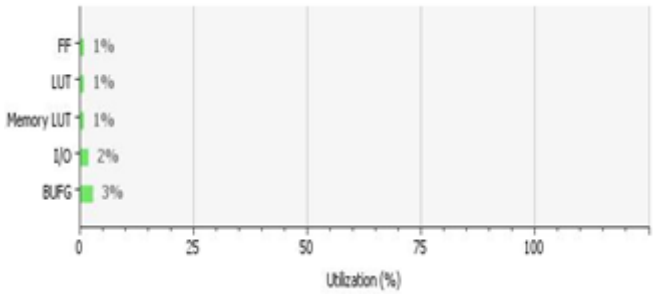

Fig.5. Post-implementation utilization in project summary

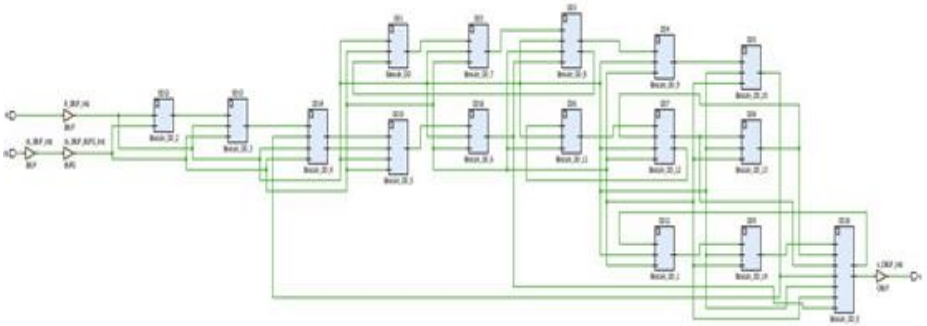

Fig.6. Schematic generated in Vivado

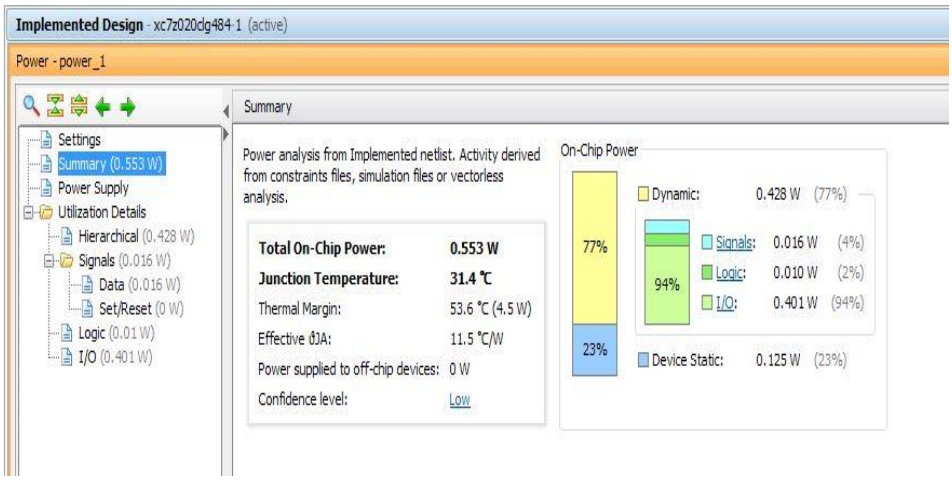

Fig.7. Summary with results from the power analysis of Kasami pseudo-random sequence generator, implemented on XC7Z020CLG484-1 circuit.

4.2. Estimation of the Power Consumption of a USRP-Based Realisation of a Communication System

The estimation of the power consumption of an USRP-based system can be done from datasheets of the device. Usually these data indicate the maximal power consumption in the aim to inform the user for the safe power supply of the USRP. The estimate in the datasheet is done by taking the worst-case values and in case of full load when all components are running at maximal power.

Table 1. Specification of the power consumption of Ettus N2x0 from [8]

Spec	Typ.	Unit
POWER		
DC Input	6	V
Current Consumption	1.3	A
w/ WBX Daughterboard	2.3	A

There is one datasheet for N2x0, although USRP N210 (see Table 1) contains a bigger FPGA - Xilinx Spartan 3A DSP - XC3SD3400A FPGA than USRP N200 which contains Xilinx Spartan 3A DSP1800 FPGA. Based on the given values for the voltage and the current, the power can be calculated as:

$$P = U*I \text{ [W]} \qquad (3)$$

For different daughterboards, power consumption is different: for the daughterboard WBX, the power consumption is 13.8 W and for the daughterboard Basic RX/TX the power consumption is 7.8 W.

For observing the USRP in GNU Radio [10] a simple flowgraph of a receiver with USRP, which receives the signal and a bloc FFT Sink for visualizing it is designed as shown on Fig.8. The process from the flowgraph in GNU Radio Companion (development of source code in Phyton, describing the flowgraph processing) takes 44 % from the CPU resources. The tool *Gnome System Monitor* [11] gives such information, after being installed and started as an application, as shown on Fig. 9.

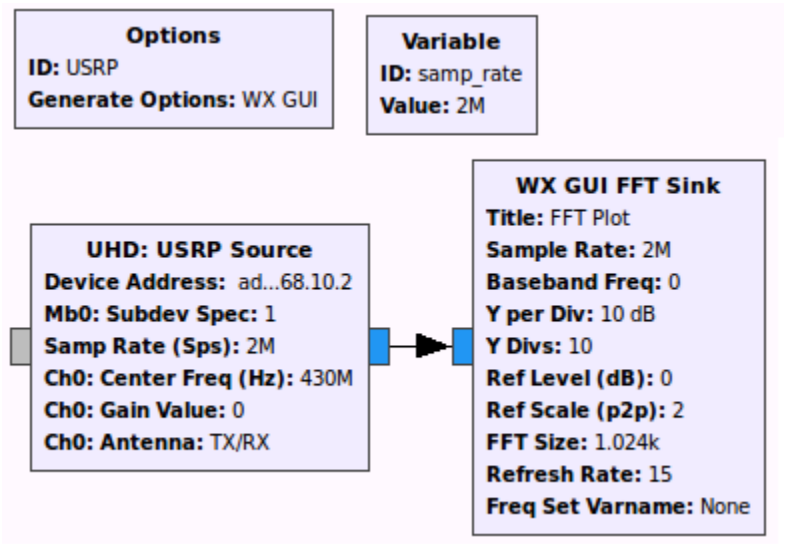

Fig.8. Flowgraph in GNU Radio of a receiver with USRP, which receives the signal and a bloc FFT Sink for visualizing it

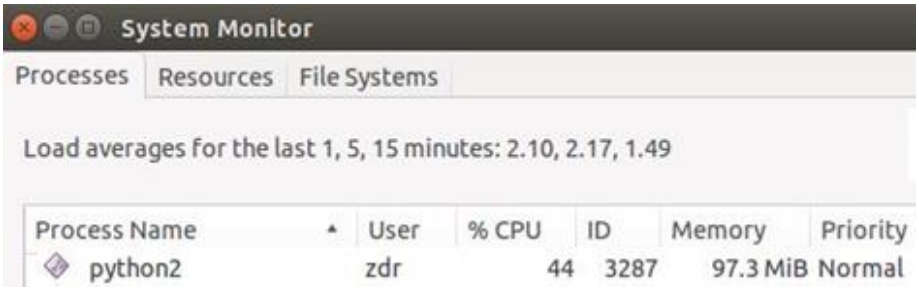

Fig.9. Information given from the tool Gnome System Monitor

P**owerstat -** Power Consumption Calculator for Ubuntu Linux [12] is a specialized tool for calculation of power consumption of components in mobile devices. Once started, it follows the system for about 10 seconds and repeats it again 48 times. The samples collected are for more than 480 seconds. While running, it displays information as: Time – when the monitoring is started, User, Nice – special value, which is priority of processing time for applications, Sys – processor load, Idle - for sleeping mode, Watts - it displays the current power consumption (energy units per second) as shown on Fig. 10.

```
gayan@gayan-Vostro-V131:~$ sudo powerstat -d 2
Running for 470 seconds (47 samples at 10 second intervals).
ACPI battery power measurments will start in 2 seconds time

  Time    User  Nice   Sys  Idle    IO  Run Ctxt/s  IRQ/s Fork Exec Exit  Watts
15:01:05   2.1   0.0   2.5  95.3   0.1    1   3435   2050    0    0    0  18.10
15:01:15   1.7   0.0   1.3  96.9   0.1    3    690    658    0    0    0  18.38
15:01:25   4.9   0.0   1.6  93.5   0.0    1   1289   1040    0    0    0  19.34
15:01:35   8.3   0.0   5.3  86.2   0.3    1   9342   5138    1    0    0  19.06
15:01:45   5.1   0.0   0.9  94.0   0.0    1   1286   1069    0    0    0  19.49
```

Fig.10. Results generated from Powerstat

After collecting the samples, the calculator gives the values "Average", "Minimum" and "Maximum" for each domain. The summary gives the "Average" percent power consumption together with the standard deviation value for a period of 480 seconds, as shown on Fig.11.

```
 Average   7.4   0.1   1.6  90.1   0.9  1.6 1670.3 1150.0  20.10
  StdDev   5.3   0.3   1.0   6.8   1.0  0.7  930.6  494.9   2.80
-------- ----- ----- ----- ----- ----- ---- ------ ------ ------
 Minimum   0.2   0.0   0.1  81.0   0.0  1.0  279.4  333.1  17.01
 Maximum  15.7   1.5   3.9  99.6   3.7  3.0 3084.1 1848.8  28.40
-------- ----- ----- ----- ----- ----- ---- ------ ------ ------
Summary:
 20.10 Watts on Average with Standard Deviation 2.80
```

Fig.11. Results from the calculator

Conclusion

The study in this paper shows that recently several methods were proposed for power consumption estimation and reduction at different stages of the communication system design. Providers and developers have answered to the increasing interest of designers to green communications by offering a set of tools and options in CAD systems to allow power consumption estimation. Tools are available in analog, analog/digital and digital design for FPGA implementation. Operational systems as Microsoft and Linux offer free power meter tools which allow determining the power consumption of device components. Two practical examples are given in the paper for power estimation of communication system design on FPGA and USRP platforms. Further research is foreseen on low power optimization of communication system design on both platforms.

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